# Type-4 2-D Diagonal and Four-Fold Rotational Symmetry Digital Filter Architectures 

Lan-Da Van, Tsung-Che Lu, Pei-Yu Chen Department of Computer Science, National Chiao Tung University, Hsinchu, Taiwan e-mail: Idvan@cs.nctu.edu.tw ; tclu@cs.nctu.edu.tw

Hari C. Reddy<br>Department of Elecrical Engineering, California State<br>University, Long Beach, USA<br>e-mail: hreddy@csulb.edu


#### Abstract

In this paper, Type-4 two-dimensional (2-D) separable denominator IIR filter architecture is studied. This structure has a critical path of one multiplication and three additions. Using this Type-4 2-D separable denominator IIR filter architecture, three new 2-D IIR filter structures with diagonal and four-fold rotational symmetries are given. These structures have a critical path of one multiplication and four additions. Further, using a different coefficient constraint, a new Type-3 2-D diagonal symmetry IIR filter architecture with a critical path of one multiplication and two additions is obtained. In all, four different 2-D IIR filter architectures with diagonal and four-fold rotational symmetries are presented.


## I. Introduction

Two-dimensional (2-D) digital filters have been extensively studied for a variety of digital signal processing (DSP) applications such as frequency response analysis [1-3], image processing [4] and beamformer [5]. To enhance the speed performance, the existing application-specific integrated circuit (ASIC) approach [3, 4, 6, 7] has been applied to design 2-D conventional filter architectures. Taking advantage of an ASIC approach, the filter designs can achieve high throughput performance and low cost. Utilizing symmetry features presented in the magnitude function of the frequency response, the number of multipliers can be reduced in ASIC implementation. Previously, Type-1 [11, 16] and Type-2 [11] and Type-3 [12, 14-16] 2-D filter architectures have been addressed. In this paper, Type-4 2-D IIR filter architectures with diagonal and fourfold rotational symmetry are explored. Also, Type-3 2-D diagonal symmetry IIR filter architecture with a different coefficient constraint that is not studied earlier is presented. The paper is organized as follows: Section II presents Type-4 2-D separable denominator IIR filter architecture. Two Type-4 and one Type-3 2-D diagonal symmetry IIR filter architectures are discussed in Section III. Next, in Section IV, one new Type-4 2-D IIR filter architecture with four-fold rotational symmetry is given. In Section V, the concise comparison in terms of critical path,
number of multiplies, the number of registers is addressed. The conclusions are given in Section VI.

## II. Type-4 2-D Separable Denominator Filter

The general transfer function of a 2-D IIR quarter-plane digital filter can be represented as follows [11, 16]

$$
\begin{equation*}
H\left(z_{1}, z_{2}\right)=\frac{Y\left(z_{1}, z_{2}\right)}{X\left(z_{1}, z_{2}\right)}=\frac{\sum_{i=0}^{N_{1}} \sum_{j=0}^{N_{2}} a_{i j} z_{1}^{-i} z_{2}^{-j}}{1-\sum_{i=0}^{N_{1}} \sum_{j=0}^{N_{2}} b_{i j} z_{1}^{-i} z_{2}^{-j}} \tag{1}
\end{equation*}
$$

where $\mathrm{X}\left(z_{1}, z_{2}\right)$ and $\mathrm{Y}\left(z_{1}, z_{2}\right)$ denote the input and output of the filter, respectively, $a_{i j}$ and $b_{i j}$ denote the numerator and denominator coefficients, respectively, and $b_{00}=0, N_{1} \times N_{2}$ is the order of the IIR filter. Considering the separable denominator transfer function, (1) can be recast as (2) [11, 16]:
$H\left(z_{1}, z_{2}\right)=\frac{Y\left(z_{1}, z_{2}\right)}{X\left(z_{1}, z_{2}\right)}=\frac{\sum_{i=0}^{N_{1}} \sum_{j=0}^{N_{2}} a_{i j} z_{1}^{-i} z_{2}^{-j}}{\left(1-\sum_{i=1}^{N_{1}} b_{i 0} z_{1}^{-i}\right) \cdot\left(1-\sum_{j=1}^{N_{2}} b_{0 j} z_{2}^{-j}\right)}$
Without loss of generality, $N_{I}=N_{2}=N$ is assumed for the filter order throughout this paper. Since $M$-size input zero-padding image signal is fed to the following filter architecture in rowscan mode, thus the delay $z_{2}^{-I}=z^{-1}$ and $z_{1}^{-1}=z^{-M}$, where $z^{-1}$ and $M$ denote a unit delay element and the width of input image with zero padding, respectively. Through the transfer function adjustment in (3), (4), and (5), the Type-4 separable denominator architecture in Fig. 1 can be obtained.

$$
\begin{equation*}
H\left(z_{1}, z_{2}\right)=\frac{Y\left(z_{1}, z_{2}\right)}{Y_{4}\left(z_{1}, z_{2}\right)} \cdot \frac{Y_{4}\left(z_{1}, z_{2}\right)}{X\left(z_{1}, z_{2}\right)} \tag{3}
\end{equation*}
$$

Assume $X=X\left(z_{1}, z_{2}\right), Y_{4}=Y_{4}\left(z_{l}, z_{2}\right)$, and $Y=Y\left(z_{l}, z_{2}\right)$ and then

$$
\begin{equation*}
Y=Y_{4}+\sum_{i=1}^{N} b_{i o} z_{1}^{-i} Y \tag{4}
\end{equation*}
$$

Therefore, $Y_{4}\left(z_{1}, z_{2}\right) / X\left(z_{1}, z_{2}\right)$ is generally expressed as

$$
\begin{equation*}
Y_{4}=\sum_{i=0}^{N} \sum_{j=0}^{N} a_{i j} z_{1}^{-i} z_{2}^{-j} X+\sum_{j=1}^{N} b_{0 j} z_{2}^{-j} Y_{4} \tag{5}
\end{equation*}
$$

It can be observed that Eq. (4) and Eq. (5) are mapped to Block 1 and Block 2, respectively. Using the tree method mentioned in [7] to arrange the adders, the critical period for the Type-4 2-D filter architecture is $T_{m}+3 T_{a}$, where $T_{m}$ and $T_{a}$ denote the operation time required by one multiplier and one adder.


Fig. 1. Type-4 2-D separable denominator IIR filter architecture for $N=3$.

## III. Proposed Type-4 and Type-3 2-D Diagonal SyMmetry IIR Filter Architectures

A 2-D magnitude response possesses diagonal symmetry if $\left|H\left(z_{1}, z_{2}\right)\right|=\left|H\left(z_{2}, z_{1}\right)\right|$ with $z_{1}=e^{j \theta_{1}}$ and $z_{2}=e^{j \theta_{2}}, \forall\left(\theta_{1}, \theta_{2}\right)$
[8]. Assume the separable denominator transfer function in (2) is adopted, it will have diagonal symmetry if $a_{i j}=a_{j i}$ and $b_{k 0}=b_{0 k}$ for all $i, j, k$. Applying these constraints to the transfer function in (2), Eqs. (4) and (5) can be recast in (6a) and (6b), respectively.

$$
\begin{gather*}
Y=Y_{4}+\sum_{j=1}^{N} b_{o j} z_{1}^{-j} Y  \tag{6a}\\
Y_{4}=\sum_{i=0}^{N} a_{i i} z_{1}^{-i} z_{2}^{-i} X+\sum_{i=0}^{N-1} \sum_{j=i+1}^{N} a_{i j}\left(z_{1}^{-i} z_{2}^{-j}+z_{1}^{-j} z_{2}^{-i}\right) X+\sum_{j=1}^{N} b_{0 j} z_{2}^{-j} Y_{4} \tag{6b}
\end{gather*}
$$

For highlighting the architecture difference compared with the previously published symmetry filter architectures, $N=3$
is selected in the following proposed filter architectures. Mapping (6a) and (6b) with $N=3$, the 2-D diagonal symmetry IIR filter architecture with separable denominator is depicted in Fig. 2. Using the tree method mentioned in [7] to arrange the adders, the critical path is analyzed as $T_{m}+4 T_{a}$ as shown in Fig. 2. It can be shown that another coefficient constraint $a_{i j}=a_{(N-j)(N-i)}$ and $b_{k 0}=b_{0 k}$ for all $i, j, k$ will also result in the diagonal symmetry. This constraint is being studied for the first time for the development of an alternate structure with diagonal symmetry. Applying these constraints to the transfer function in (2), Eq. (5) can be recast in (7).

$$
\begin{align*}
& Y_{4}=\sum_{i=0}^{N} a_{i(N-i)} z_{1}^{-i} z_{2}^{-(N-i)} X  \tag{7}\\
& +\sum_{i=0}^{N-1} \sum_{j=0}^{N-i-1} a_{i j}\left(z_{1}^{-i} z_{2}^{-j}+z_{1}^{-(N-j)} z_{2}^{-(N-i)}\right) X+\sum_{j=1}^{N} b_{0 j} z_{2}^{-j} Y_{4}
\end{align*}
$$

The corresponding Type-4 2-D diagonal symmetry IIR filter architecture is shown in Fig. 3. For completeness, the Type-3 2-D diagonal symmetry IIR filter architecture derived from the main equation (8) with $a_{i j}=a_{(N-j)(N-i)}$ is shown in Fig. 4.

$$
\begin{align*}
& Y_{3}=\sum_{i=0}^{N} a_{i(N-i)} z_{1}^{-i} z_{2}^{-(N-i)} X  \tag{8}\\
& +\sum_{i=0}^{N-1} \sum_{j=0}^{N-i-1} a_{i j}\left(z_{1}^{-i} z_{2}^{-j}+z_{1}^{-(N-j)} z_{2}^{-(N-i)}\right) X+\sum_{j=1}^{N} b_{0 j} z_{1}^{-j} Y_{3}
\end{align*}
$$



Fig. 2. Type-4 2-D diagonal symmetry IIR filter architecture with $a_{i j}=a_{j i}$ for $N=3$.


Fig. 3. Type-4 2-D diagonal symmetry IIR filter architecture with $a_{i j}=a_{(N-j)(N-i)}$ for $N=3$.


Fig. 4. Type-3 2-D diagonal symmetry IIR filter architecture with $a_{i j}=a_{(N-j)(N-i)}$ for $N=3$.

## IV. Proposed Type-4 2-D Four-Fold Rotational Symmetry IIR Filter Architecture

For a 2-D magnitude response, if $\left|H\left(z_{1}, z_{2}\right)\right|=\left|H\left(z_{2}^{-1}, z_{1}\right)\right|$ with $z_{1}=e^{j \theta_{1}}$ and $z_{2}=e^{j \theta_{2}}, \forall\left(\theta_{1}, \theta_{2}\right)$, the filter possesses four-fold rotational symmetry. With the separable denominator transfer function in (2), the following constraints on the coefficients will provide the required symmetry: $a_{i j}=a_{j(N-i)}$ and $b_{k 0}=b_{0 k}$ for all $i, j, k$. Applying these constraints to the transfer function in (2), Eqs. (4) and (5) can be recast in (9a) and (9b), respectively.

$$
\begin{align*}
& \quad Y=Y_{4}+\sum_{j=1}^{N} b_{o j} z_{1}^{-j} Y  \tag{9a}\\
& Y_{4}=v a_{u u} z_{1}^{-u} z_{2}^{-u} X \\
& +\sum_{i=0}^{u-v} \sum_{j=i}^{N-i-1} a_{i j}\left(z_{1}^{-i} z_{2}^{-j}+z_{1}^{-j} z_{2}^{-(N-i)}+z_{1}^{-(N-i)} z_{2}^{-(N-j)}+z_{1}^{-(N-j)} z_{2}^{-i}\right) X \\
& +  \tag{9b}\\
& +\sum_{j=1}^{N} b_{0 j} z_{2}^{-j} Y_{4}
\end{align*}
$$

where $u=\lfloor N / 2\rfloor$ and $v=(N+1) \bmod 2$. Note that $\lfloor\bullet\rfloor$ denotes the largest integer that is smaller than or equal to • . In the case of $N=3$, ( 9 a ) and ( 9 b ) can be realized as 2-D four-fold rotational symmetry IIR filter architecture in Fig. 5. Using the tree method to arrange the adders, the critical path is analyzed as $T_{m}+4 T_{a}$ as shown in Fig. 5.


Fig. 5. Type-4 2-D four-fold rotational symmetry IIR filter architecture for $N=3$.

## V. Comparison

The comparison results in terms of critical path, number of multiplies, the number of registers are shown in Table 1. It is interesting to note that Type 4 separable denominator IIR filter architecture has $T_{m}+3 T_{a}$, but the diagonal symmetry and
four-fold rotational IIR filter architectures have longer critical path $T_{m}+4 T_{a}$. The proposed Type-3 2-D diagonal symmetry IIR filter architecture has the same good performance (i.e., lowest critical path) as Type-2 and Type-3 2-D IIR filter architectures. In terms of number of multipliers, Type-4, Type-1, Type-2 and Type-3 2-D IIR filter architectures possess fewer multipliers than conventional 2-D IIR filter architecture [7] due to the use of symmetry property. In terms of the number of registers, Type-4 2-D IIR filter architecture has the largest register account.

## VI. Conclusion

Three new Type-4 2-D IIR filter architectures using diagonal and four-fold symmetries and one new Type-3 2-D IIR filter architecture using diagonal symmetry are proposed. Most importantly, Table 1 among four types 2-D IIR filter architectures provides a complete comparison such that the users can easily select a suitable filter architecture for the practical application.

## ACKNOWLEDGEMENT

The authors would like to thanks the supports of MOST 106-2221-E-009-028-MY3 and MOST 106-2218-E-009-029.

## REFERENCES

[1] D. E. Dudgeon and R. M. Mersereau, Multidimensional Digital Signal Processing. Englewood Cliffs, NJ: Prentice-Hall, 1984.
[2] A. V. Oppenheim and R. W. Schafer, Discrete-Time Signal Processing, Englewood Cliffs, NJ: Prentice-Hall, 1989, chapter 6.
[3] W. S. Lu and A. Antoniou, Two-Dimensional Digital Filters. Marcel Dekker, Inc. New York, NY, USA 1992, chapter 11.
[4] M. A. Sid-Ahmed, Image Processing: Theory, Algorithms, and Architectures. NY: McGraw-Hill, 1995.
[5] A. Madanayake, C. Wijenayake, D. G. Dansereau, T. K. Gunaratne, L. T. Bruton, and S. B. Williams, "Multidimensional (MD) circuits and systems for emerging applications including cognitive radio, radio astronomy, robot vision and imaging", IEEE Circuits and Systems Magazine, vol. 13, no. 1, pp. 10-43, 2013.
[6] N. R. Shanbhag, "An improved systolic architecture for 2-D digital filters," IEEE Trans. Signal Processing, vol. 39, no. 5, pp. 1195-1202, May 1991.
[7] L. D. Van, "A new 2-D systolic digital filter architecture without global broadcast," IEEE Trans. VLSI Syst., vol. 10, no. 4, pp. 477-486, Aug . 2002
[8] H. C. Reddy, I. H. Khoo and P. K. Rajan, "2-D symmetry: theory and filter design applications," IEEE Circuits and Systems Magazine, vol. 3, pp. 4-33, 2003.
[9] P. Y. Chen, L. D. Van, H. C. Reddy and C. T. Lin, "A new VLSI 2-D diagonal-symmetry filter architecture design," in Proc. IEEE APCCAS, Macao, China, pp. 320-323, Nov. 2008.
[10] P. Y. Chen, L. D. Van, H. C. Reddy and C. T. Lin, "A new VLSI 2-D fourfold-rotational-symmetry filter architecture design," in Proc. IEEE ISCAS, Taiwan, pp. 93-96, May, 2009.
[11] P. Y. Chen, L. D. Van, I. H. Khoo, H. C. Reddy and C. T. Lin, "Power-Efficient and Cost-Effective 2-D Symmetry Filter Architectures," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 58, no. 1, pp. 112-125, Jan. 2011.
[12] P. Y. Chen, L. D. Van, H. C. Reddy, and I. H. Khoo, "Areaefficient 2-D digital filter architectures possessing diagonal and four-fold rotational symmetries," in Proc. International Conference on Information, Communications and Signal Processing (ICICS), Taiwan, Dec., 2013.
[13] I. H. Khoo, H. C. Reddy, L. D. Van, and C. T. Lin, "General formulation of shift and delta operator based 2-D VLSI filter structures without global broadcast and incorporation of the symmetry," Multidimensional Systems and Signal Processing, vol. 25, issue 4, pp. 795-828, Oct. 2014.
[14] P. Y. Chen, L. D. Van, H. C. Reddy, and I. H. Khoo, "New 2-D filter architectures with quadrantal symmetry and octagonal symmetry and their error analysis," in Proc. IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), pp. 265-268, Aug. 2017, Boston, USA.
[15] P. Y. Chen, L. D. Van, H. C. Reddy, and I. H. Khoo, "Type-3 2-D multimode IIR filter architecture and the corresponding symmetry filter's error analysis," in Proc. IEEE International Conference on ASIC (ASICON), Oct. 2017, pp. 265-268, Guiyang, China.
[16] L. D. Van, I. H. Khoo, P. Y. Chen, and H. C. Reddy, "Symmetry incorporated cost-effective architectures for twodimensional digital filters," IEEE Circuits and Systems Magazine, accepted to be published in 2018.

Table 1: Comparison Results among Four Types 2-D IIR Filters Architectures.

| Type |  | Critical Path | \# of Multipliers for $N=3$ | \# of Registers for $N=3$ |
| :---: | :---: | :---: | :---: | :---: |
| Van [7] |  | $T_{m}+3 T_{a}$ | 31 | $3 \mathrm{M}+23$ |
| Type-1 | Separable Denominator | $T_{m}+3 T_{a}$ | 22 | $3 \mathrm{M}+18$ |
|  | Diagonal |  | 16 | $3 \mathrm{M}+23$ |
|  | Four-fold |  | 10 | $3 \mathrm{M}+24$ |
| Type-2 | Separable Denominator | $T_{m}+2 T_{a}$ | 22 | $3 \mathrm{M}+17$ |
|  | Diagonal |  | 16 | $3 \mathrm{M}+23$ |
|  | Four-fold |  | 10 | $3 \mathrm{M}+24$ |
| Type-3 | Separable Denominator | $T_{m}+2 T_{a}$ | 22 | $3 \mathrm{M}+18$ |
|  | Diagonal with $a_{i j}=a_{j i}$ |  | 16 | $3 \mathrm{M}+24$ |
|  | Diagonal with $a_{i j}=a_{(N-j)(N-i)}$ (This work) |  | 16 | $3 \mathrm{M}+30$ |
|  | Four-fold |  | 10 | $3 \mathrm{M}+25$ |
| Type-4 (This work) | Separable Denominator | $T_{m}+3 T_{a}$ | 22 | $6 \mathrm{M}+14$ |
|  | Diagonal with $a_{i j}=a_{j i}$ | $T_{m}+4 T_{a}$ | 16 | $6 \mathrm{M}+20$ |
|  | Diagonal with $a_{i j}=a_{(N-j)(N-i)}$ |  | 16 | $6 \mathrm{M}+26$ |
|  | Four-fold |  | 10 | $6 \mathrm{M}+21$ |

