An Efficient Systolic Architecture for the DLMS Adaptive Filter and Its Applications

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***Abstract*—In this paper, we propose an efficient systolic architecture for the delay least-mean-square (DLMS) adaptive finite impulse response (FIR) digital filter based on a new tree-systolic processing element (PE) and an optimized tree-level rule. Applying our tree-systolic PE, a higher convergence rate than that of the conventional DLMS structures can be obtained without sacrificing the properties of the systolic-array architecture. The efficient systolic adaptive FIR digital filter not only operates at the highest throughput in the word-level but also considers finite driving/update of the feedback error signal. Furthermore, based on our proposed optimized tree-level rule that takes account of minimum delay and high regularity, an efficient N-tap systolic adaptive FIR digital filter can be easily determined under the constraint of maximum driving of the feedback error signal.**

***Index Terms*—Adaptive filter, DLMS algorithm, equalization, system identification, systolic architecture.**

I. Introduction

ADAPTIVE digital filters have a wide range of communication and DSP applications such as adaptive equalization [1], system identification [2], and image restoration [3]. The most widely used algorithm for adaptive filters is the least-mean-square (LMS) algorithm [4] due to its superior performance and simple calculation. The LMS algorithm is well suited to software-based simulation and analysis but is not applicable to hardware implementation. Thus, Long *et al.* [5], [6] developed and studied the characteristics of the DLMS algorithm such that the VLSI design of an approximate LMS adaptive finite impulse response (FIR) digital filter could be possible. In order to reduce the delay value, a tree-structure is first provided and applied in [5]; however, there exist driving, modularity, and local connection problems because the feedback error term needs to concurrently drive/update all the weights of the adaptive digital filter. In view of hardware design, finite driving/update eliminates the fan-out problem. Modularity is advantageous within a high regularity system such as an adaptive FIR digital filter since the layout of a module can be duplicated and reused, and the accurate timing sequence of the whole system can be easily checked. On the other hand, when a large number of PEs work together, local data communication becomes more significant since global connection impacts upon speed, power, and area [18]–[20]. Owing to the limitation of maximum driving of the feedback error signal and the requirement of modularity and local connection in the hardware, it is difficult to directly implement the DLMS algorithm without considering systolic techniques [17]–[20]. Thus, much research [7], [8] has been conducted on the use of a systolic array architecture for the DLMS adaptive FIR digital filter. Generally speaking, the delay value is either equal to N within the conventional systolic-array architecture [7], [8] or lower than N by the tree method that takes no account of systolic arrays [5], [6]. Recently, Douglas *et al.* [9] and Matsubara *et al.* [11] proposed new structures that apply the technique [12], which converts the DLMS algorithm into the LMS algorithm. Both structures approach well the convergence of the LMS algorithm. However, the conversion requires a larger area cost of calculating the newly derived feedback error if the convergence comes close to LMS convergence performance. As a result, we are motivated to design an efficient DLMS systolic architecture based on a newly proposed tree-systolic PE and an optimized tree-level rule for communication applications. The structure of this paper is organized as follows. In Section II, we propose a new tree-systolic PE that is a hybrid of the tree structure [5] and PEs of conventional systolic architectures [7], [8] to construct an efficient systolic adaptive FIR digital filter. In addition, an optimized rule to decide the number of tree levels is provided under the constraint of maximum driving of the feedback error signal. For convenience of comparisons, the comprehensive hardware characteristics are described and discussed in Section III. In Section IV, we verify our systolic adaptive FIR digital filter architecture via simulation of adaptive equalization [1] and system identification [2] applications. Obviously, the proposed efficient systolic architecture that maintains satisfactory convergence performance has the same lowest critical period as that in [5], finite driving/update, and high degrees of modularity and locality at no extra area cost. Finally, concise statements conclude this paper in the last section.

II. An Efficient Systolic Architecture

The LMS adaptive algorithm [4] minimizes approximately the mean-square error by recursively altering the weight vector at each sampling instance. Thus, an adaptive FIR digital filter driven by the LMS algorithm can be described in vector form as

$$y(n) = \mathbf{w}^T(n)\mathbf{x}(n) \tag{1}$$

$$e(n) = d(n) - y(n) \tag{2}$$

$$\mathbf{w}(n+1) = \mathbf{w}(n) + \mu e(n)\mathbf{x}(n) \tag{3}$$

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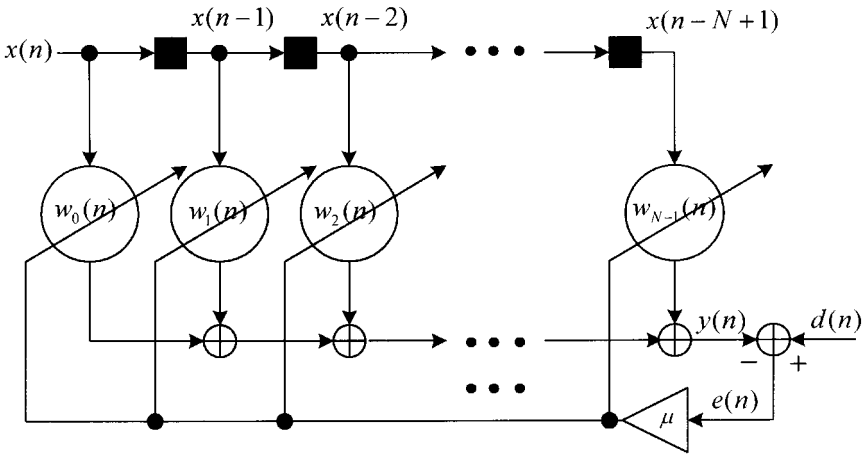

Fig. 1. Block diagram of an adaptive FIR digital filter driven by the LMS algorithm.

where $d(n)$ and $y(n)$ denote the desired signal and output signal, respectively. The step-size μ is used for adaptation of the weight vector, and $e(n)$ is the feedback error. In the above equations, the tap-weight vector $\mathbf{w}(n)$ and the tap-input vector $\mathbf{x}(n)$ are defined as

$$\mathbf{w}(n) = [\omega_0(n), \omega_1(n), \ldots, \omega_{N-1}(n)]^T$$
$$\mathbf{x}(n) = [x(n), x(n-1), \ldots, x(n-N+1)]^T$$

where N is the length of an FIR digital filter and $[\bullet]^T$ denotes the transpose operator. The block diagram of the LMS adaptive FIR digital filter is depicted in Fig. 1, where the symbol ■ denotes the unit delay element. The coefficient update using the DLMS algorithm [5] of an N-tap adaptive FIR digital filter is represented by the following equation:

$$\mathbf{w}(n+1) = \mathbf{w}(n) + \mu e(n-D)\mathbf{x}(n-D) \tag{4}$$

where D is the delay value in weight adaptation. In the following, we will focus on reducing the delay value D, obtaining low critical period (i.e., high throughput), and satisfying the requirement of systolic-array realization [17]–[20], since the first results in faster convergence, the second guarantees high-speed operation, and the last implies a high degree of suitability for VLSI implementation. The critical period is defined as the minimum operation cycle time for each correct response of a digital system. Emphasizing again, we intend to design an efficient architecture mapped from (1), (2), and (4) without modifying the DLMS algorithm.

It is known that the tree method enhances the performance of adaptive FIR digital systems [5], [10], [11]. However, in [5], the tree structure lacks driving-consideration, modularity, and local-connection. In [10] and [11], while the number of tree levels increases, the critical period would be sacrificed since the pipeline is not sufficiently full. Here, we apply the tree concept to devise a new generalized tree-systolic processing element, PE_p, as shown in Fig. 2(a), where we insert unit delay elements marked with hatching. The PE_p combines the merits of the tree structure [5] and systolic architecture [7], [8] to reduce the value of D, and achieve modularity, local connection, as well as the lowest critical period. The subscript p of PE_p denotes the number of tree levels, where $p \in \{0, N^+\}$ in which N^+ denotes a set of positive integers. Note that $p \leq p_{\max}$, where the value of $p_{\max}$ is based on maximum driving capability of the feedback error signal. The maximum driving, which can be estimated from design parameters [15], [16], can be quantified as the maximum number of tap-connections. Note that the design parameters involve the desired critical period, operating voltage, aspect ratio, and logic style. Let the maximum number of tap-connections of the feedback error signal be just larger than or equal to the value $2^{p_{\max}}$ to achieve a high degree of reliability and convenient processing. Thus, $p_{\max}$ can be obtained. For example, PE_2 depicted in Fig. 2(b) represents the case that the maximum driving of the feedback error signal is equal to $2^2 = 4$ tap-connections per clock cycle. Hence, unlike the structure [5], this new PE leads to a high degree of realization due to finite driving/update, modularity, and local connection. Also, this new PE operates at the highest throughput and with local connection, unlike the structure [11]. Although we have proposed a similar PE in [13], that PE cannot be exactly mapped to the weight update equation, (4), so we modified it to obtain Fig. 2(a) [14]. Now, many types of PE_p for $p = 0, 1, 2, \ldots, p_{\max}$ can be obtained to construct an N-tap adaptive FIR digital filter. The resulting highly realizable systolic architecture of the DLMS adaptive digital filter is depicted in Fig. 3, where z^{-1} denotes a unit delay. In Fig. 3, we insert a unit delay element ■ in the feedback path so as to maintain the lowest critical period. Fortunately, we find that there are many choices to construct an N-tap systolic adaptive FIR digital filter at a different initial value p. How to choose PE_p can be solved with an optimized tree-level rule to be described later. We observe that when p is equal to zero, this architecture can be reduced to a fully pipelined architecture as in [7], [8]. On the other hand, if p is greater than zero, this architecture performs better convergence than that in [7], [8] without sacrificing systolic features. Moreover, the same lowest period as that in [5] can be achieved among proposed structures.

Next, let us explain how to choose the tree level under the constraint of maximum driving of the feedback error signal. Before deciding the value of p, we must investigate the relationship for D versus p, and N_p versus p, where N_p denotes the required number of different kinds of PEs at each p. It is known

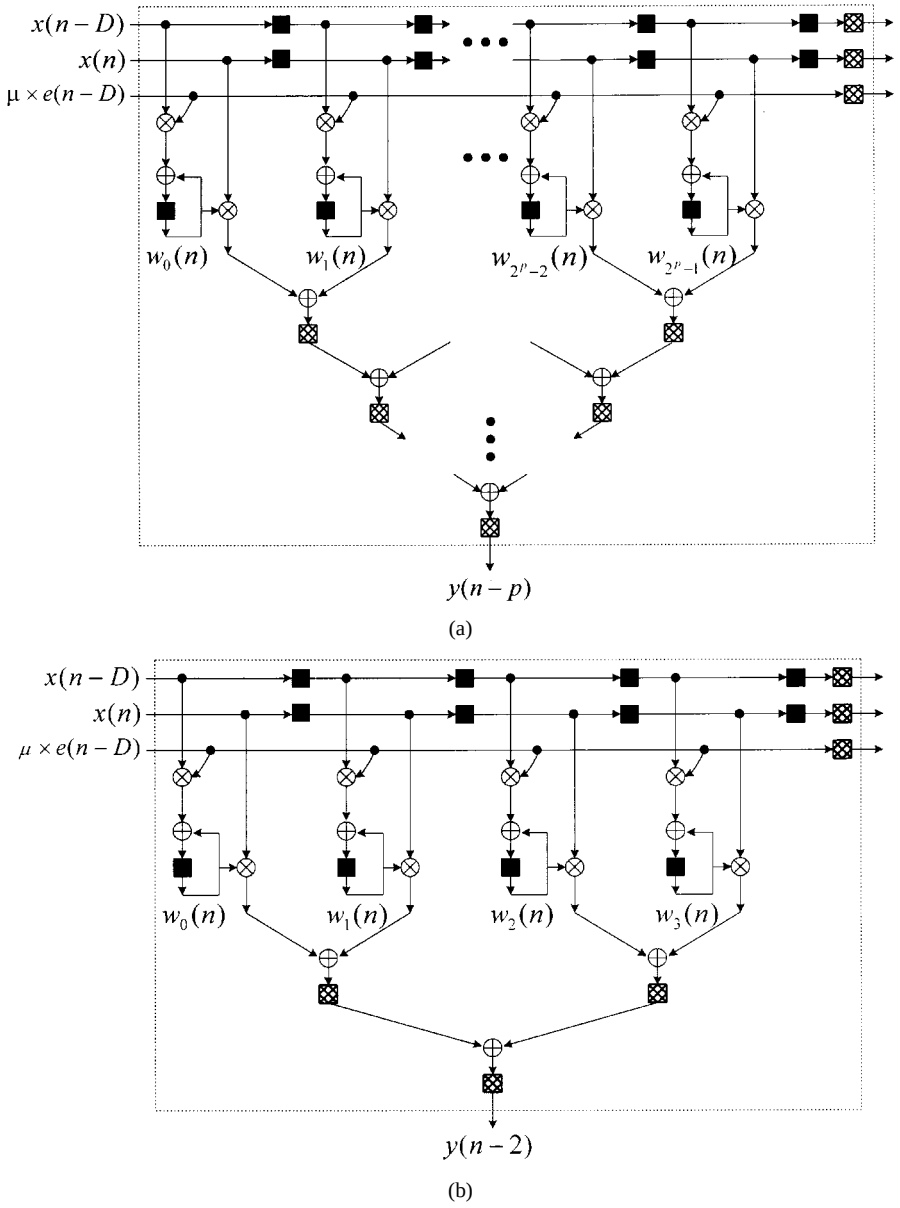

Fig. 2. (a) A new generalized tree-systolic processing element PE_p constructed by inserting delay elements marked with hatching. (b) An example of PE_2.

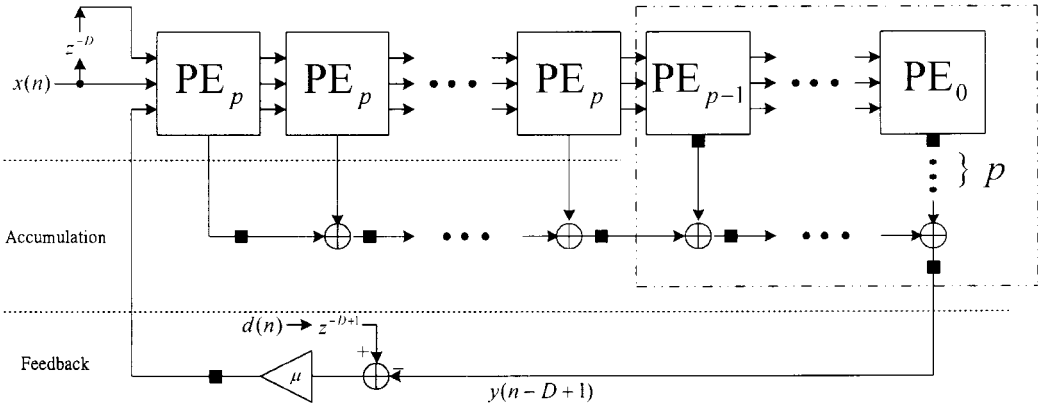

Fig. 3. Overall systolic architecture with cascaded tree-systolic PEs.

that the two performance indices D and N_p affect the convergence rate and the number of different kinds of PEs (i.e., regularity), respectively. Emphasizing again, the lower bound and upper bound of p are zero and $p_{\max}$, respectively. For convenience of simulation for D versus different values p, we use D_p instead of D. Each PE_p as shown in Fig. 2(a) has 2^p taps and

the delay value p from $x(n)$ to $y(n-p)$. According to our efficient N-tap systolic adaptive architecture as shown in Fig. 3, the number of PE_ps is $\lfloor N/2^p \rfloor$, where $\lfloor \bullet \rfloor$ indicates the maximum integer value less than or equal to $\bullet$. $2^p \times \lfloor N/2^p \rfloor$ subtracted from N gives the number of residual taps that is less than 2^p. If the number of residual taps is equal to zero, we calculate the delay value D_p and stop to proceed with the next value of p. Otherwise, we choose an appropriate PE whose number of taps is just less than or equal to the number of residual taps. After the number of taps of the above appropriate PE is subtracted from the number of residual taps, a new number of residual taps can be obtained. If the new number of residual taps is equal to zero, we calculate the delay value D_p and stop to proceed with the next value of p. Otherwise, we follow a similar procedure to find the next cascaded PE until the final number of residual taps is equal to zero. The delay value D_p can be obtained by summing up three terms: the delay value p of the PE_p, one unit delay in the feedback path, and the number of all cascaded PEs in Fig. 3. On the other hand, the value of N_p increases in the following two cases. One is that the new number of residual taps is equal to zero. The other case is that the new number of residual taps is larger than zero, and the previous and the new numbers of residual taps are not equal. Therefore, the rule corresponding to the above description can be programmed as

Rule:

for $p = 0{:}\ 1{:}\ p_{\max}$
  $N_p = 1$; $t_p = p$;
  $S_p = N \bmod 2^p$;
  if $(S_p == 0)$

$$D_p = p + 1 + \left\lfloor \frac{N}{2^p} \right\rfloor;$$

  else
    for $k = (p-1){:}\ -1{:}\ 0$
      $S_k = S_{k+1} \bmod 2^k$;
      $t_p = t_p - 1$;
      if $(S_k == 0)$
        $N_p = N_p + 1$;

$$D_p = p + 1 + \left\lfloor \frac{N}{2^p} \right\rfloor + \sum_{t=t_p}^{p-1} \left\lfloor \frac{S_{t+1}}{2^t} \right\rfloor;$$

        break;
      else
        if $(S_k > 0 \,\&\, S_k == S_{k+1})$
          $N_p = N_p$;
        else
          $N_p = N_p + 1$;
        end
      end
    end
  end
end

where the notation $k = a{:}b{:}c$ denotes that k starts from a and ends at c with an increment of b, where a, b, and c belong to an integer set. The two integer parameters t_p and S_k indicate the initial value of the variable t and the kth number of residual taps obtained from the modulus operator (mod), respectively. The relational equal operator and the logical AND operator are denoted as $==$ and &, respectively. The instruction "*break*" terminates execution of the adjacent *for* loop. Obviously, we can formulate the delay value D_p versus p as

$$D_p = p + 1 + \left\lfloor \frac{N}{2^p} \right\rfloor + \sum_{k=t_p}^{p-1} \left\lfloor \frac{S_{k+1}}{2^k} \right\rfloor. \tag{5}$$

In this paper, since our objective is to obtain a minimum delay D_p, we choose the value p that leads to a minimum delay through the above rule. However, in many cases, there are several values p to result in the same D_p under the same constraint and we solve as follows. If there are two, or more than two, different values p to lead to the same D_p but different N_p, then we choose the value p with the lower/lowest N_p. If there are two, or more than two, different values p to result in the same value of $\{D_p, N_p\}$, it means that these values p are the optimized tree-level values under the constraint of maximum driving of the feedback error signal. For example, if N is equal to 62 and the maximum driving of the error signal is 32 taps per clock cycle (i.e., $p_{\max} = 5$), then the values of $\{D_p, N_p\}$as shown in Fig. 4 are equal to $\{63, 1\}$, $\{33, 1\}$, $\{19, 2\}$, $\{13, 3\}\{11, 4\}$ and $\{11, 5\}$ corresponding to $p = 0$, 1, 2, 3, 4, and 5, respectively. We observe that $p = 4$ and 5 can achieve the same minimum delay $D_p = 11$. With respect to the characteristic of the regularity, we compare the values N_p for $p = 4$ and 5, and detect that fewer kinds of PEs are required for $p = 4$. That is, we need only 4 types of PEs (i.e., PE_4, PE_3, PE_2, PE_1) to construct the efficient systolic adaptive FIR digital filter architecture. With the minimum delay and high regularity in mind, $p = 4$ is an optimized number of tree levels in this example. Therefore, the rule shows consideration for minimum delay and high regularity while varying p under the constraint of maximum driving.

As to an efficient two-dimensional (2-D) DLMS systolic adaptive digital filter, the interested readers can refer to our recent work in [14] to obtain the detailed architecture; therefore, we ignore the presentation here.

III. Comparison Results among Different Architectures

In view of hardware characteristics, we provide comprehensive comparison results for different N-tap adaptive FIR filter structures in Table I. Since D-Z-Ss' structure [9] and M-N-Ks' structure independently utilize the same conversion of the DLMS into the LMS algorithm, the proposed structures have similar characteristics. Hence, we tabulate only the features of M-N-Ks' structure while ignoring those of D-Z-Ss' structure. Note that T_m and T_a denote the operation time for one multiplication as well as one addition, respectively. The critical period has been defined in Section II. In [10] and [11], δ and r are defined as integer parameters for exhibiting the convergence characteristic and for concurrently adjusting the number of taps, respectively.

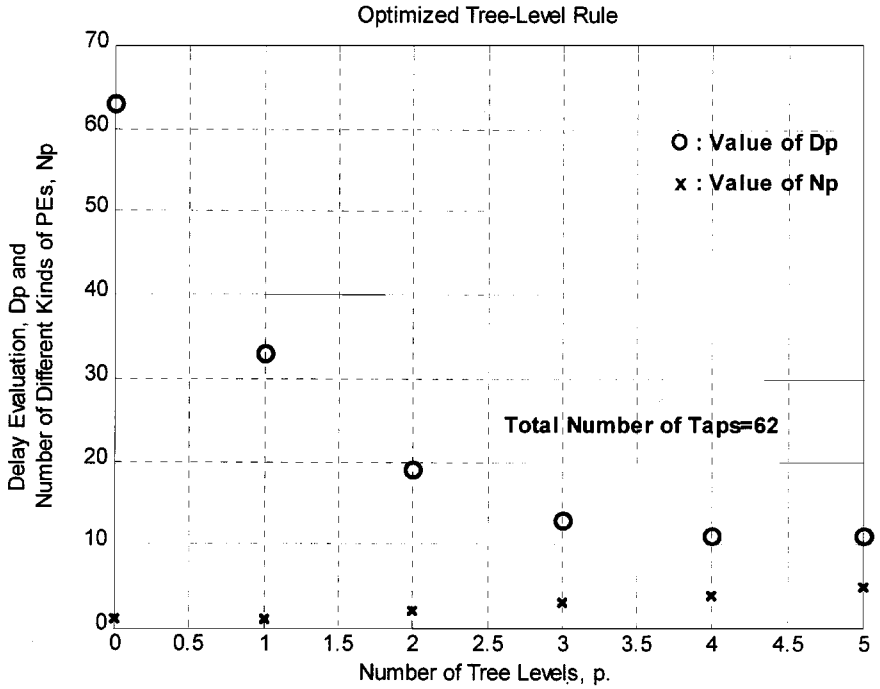

Fig. 4. An optimized tree-level rule considering minimum delay and high regularity.

TABLE I
COMPARISON RESULTS OF THE DIFFERENT N-TAP ADAPTIVE FIR FILTER ARCHITECTURES

	LMS Structure [4]	DLMS Structure [5]	M-As' and H-H-Bs' Structures [7, 8]	M-N-Ks' Structure [10, 11]	This work
Architecture Type	Nonsystolic	Nonsystolic	Systolic	Semisystolic	Systolic
Critical Period	$3T_m + (N+1)T_a$	$T_m + T_a$	$2T_m + 2T_a$	$T_m + \lceil \log_2(r+1) \rceil T_a$	$T_m + T_a$
Convergence Characteristic	Best	Depends on $\log_2 N$	Normal	Depends on δ	Depends on p
Value of D	0	$\log_2 N + 1$	N	$\left\lceil \frac{N}{r} \right\rceil + 1$	$p+1+\left\lfloor \frac{N}{2^p} \right\rfloor + \sum_{k=1_p}^{p-1} \left\lfloor \frac{S_{k+1}}{2^k} \right\rfloor$
No. of Multipliers	$2N+1$	$2N+1$	$3N$, $2N+1$	$2N+1+2\delta$	$2N+1$

The most attractive structure candidate for VLSI implementation is the systolic architecture rather than nonsystolic or semisystolic architectures. As described in Section II, our proposed architecture is certainly a systolic architecture. The LMS structure as shown in Fig. 1 is obviously a nonsystolic architecture. The DLMS structure [5] also belongs to a nonsystolic architecture due to lack of finite driving, modularity, and local connection. In [11], the structure that generates the new feedback error does not consider the finite driving and local connection for input, $x(n)$, so this structure should be classified as a semisystolic structure.

Before comparing the convergence performance, we define the convergence in [7], [8] as "normal," since the delay value D is equal to the entire tap-number N. It is well known that for a larger delay value, slower convergence could be obtained [5] unless the conversion technique [12] is used. Since the conventional systolic DLMS architectures [7], [8] require the longest delay value, the slowest convergence is expected. Now that the convergence of the LMS algorithm [4] is our aim, the convergence of the LMS structure is therefore considered to be the "best." For a convergence comparison of M-N-Ks' structure and our work, we briefly show constraints of M-N-Ks' pipeline design as

$$\delta \le D - D_B \tag{6}$$

$$D_B = \left\lceil \frac{T_m + \lceil \log_2 \delta \rceil T_a}{T_m + \lceil \log_2 (r+1) \rceil T_a} \right\rceil. \tag{7}$$

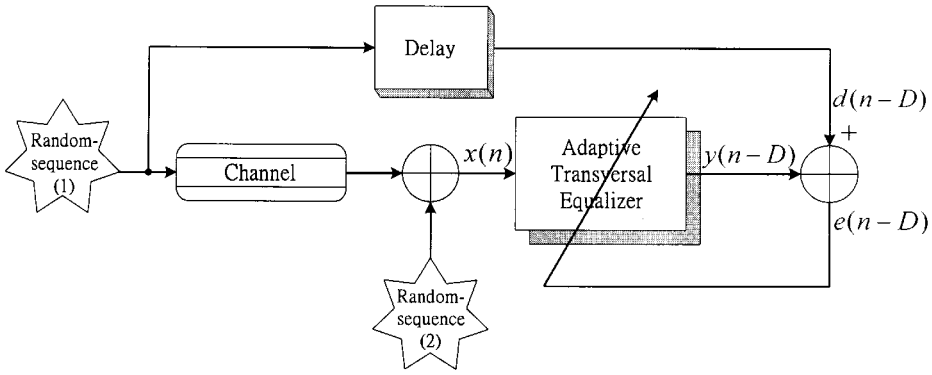

Fig. 5. Block diagram of adaptive equalization.

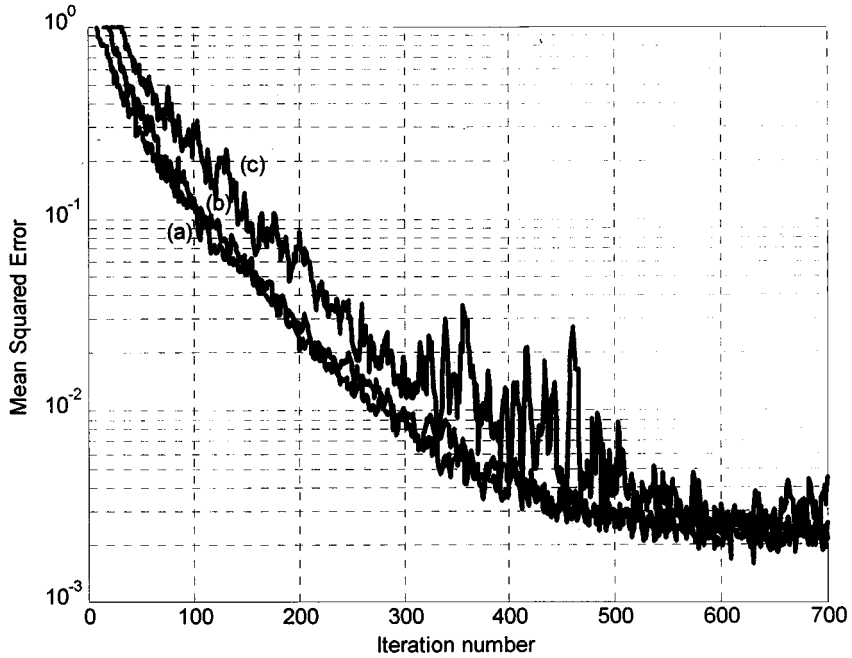

Fig. 6. Comparison results of adaptive equalization with (a) LMS structure; (b) efficient systolic DLMS structure using an optimized tree-level rule; and (c) conventional DLMS structure.

In the word-level computation, assume $T_m \gg T_a$ such that there is little effect on $D_B \cong 1$ in (7); that is, δ has a wide range to be adjusted in (6). While $\delta = D - D_B$, a good approximation to the convergence of the LMS algorithm is brought about at the expense of the number of multipliers (i.e., a higher area cost). In our paper, although a larger $p_{\max}$ is allowable, the convergence can be approximated to that of the LMS algorithm at no extra area cost.

The proposed architecture has the same critical period as that in [5] and the critical period is independent of other control parameters. When $r = 1$, M-N-Ks' structure can achieve the same critical period as that listed in our work; however, it requires a larger delay value D than our work [13], [14]. In this situation ($r = 1$), when the convergence of the LMS algorithm is desired, δ becomes larger (i.e., a higher area cost) in (6).

As shown in Table I, by using our proposed systolic architecture suitable for a single chip realization, we can furnish the lowest critical period in the word-level and better convergence without sacrificing finite-driving, area-cost, modularity, regularity, and local-connection characteristics.

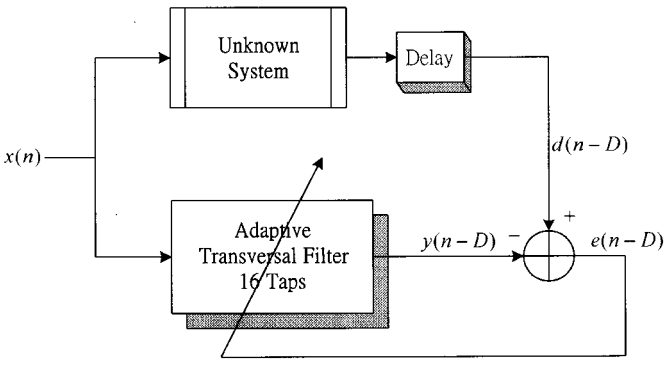

Fig. 7. Block diagram of system identification.

IV. Applications of the Efficient Systolic Adaptive Digital Filter

In this section, we simulate two applications to verify the validity of our proposed architecture and rule. Since the M-N-Ks'

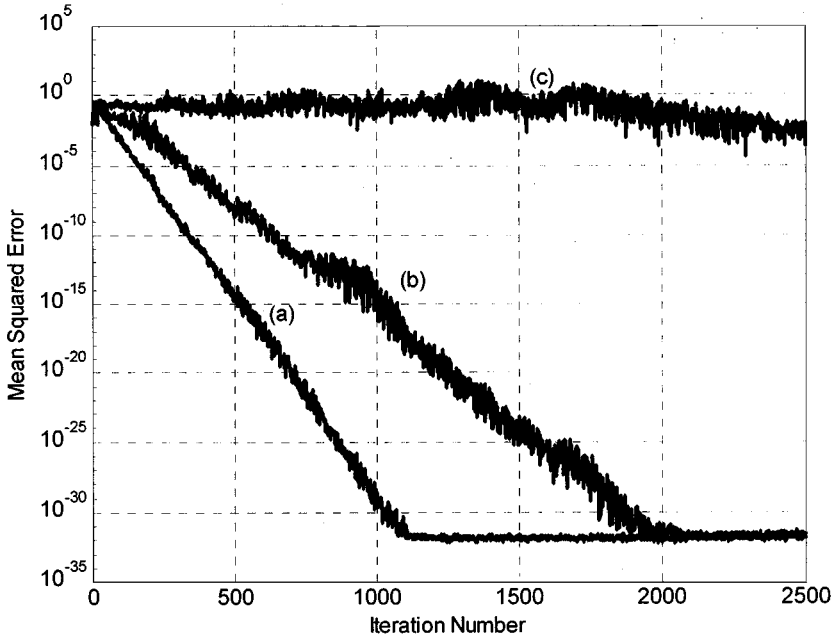

Fig. 8. Comparison results of system identification with: (a) LMS structure, (b) efficient systolic DLMS structure using an optimized tree-level rule, and (c) conventional DLMS structure.

structure, whose convergence performance depends on the selection of δ, can approximate well either the LMS or the DLMS algorithms, we ignore simulation of M-N-Ks' structure and simulate only the LMS structure, the efficient systolic DLMS structure using an optimized tree-level rule, and the conventional DLMS structure.

In the first application, we study the efficient architecture for adaptive equalization [1] as shown in Fig. 5 with a linear dispersive channel that produces unknown distortion. The adaptive equalization has the task of correcting distortion produced by the channel in the presence of the additive white noise. The random sequence 1 applied to the channel input consists of a Bernoulli sequence with zero mean and unit variance. Another random-sequence 2 that corrupts the channel output serves as the source of additive white Gaussian noise with zero mean and 10^{-3} variance. These two random sequences are independent of each other. The impulse response of the channel is modeled as the raised cosine

$$h_n = \begin{cases} \frac{1}{2}\left[1+\cos\left(\frac{2\pi}{M}(n-2)\right)\right], & n=1,\,2,\,3 \\ 0, & \text{otherwise} \end{cases} \tag{8}$$

where the parameter M controls the degree of amplitude distortion produced by the channel. Herein, we choose M, $p_{\max}$, and μ equal to 3.1, 3, and 0.027, respectively, for $N = 12$. Through the optimized tree-level rule, $p = 0$, 1, 2, and 3 result in $\{D, N_p\} = \{13, 1\}$, $\{8, 1\}$, $\{6, 1\}$, and $\{6, 2\}$, respectively, so we detect that $p = 2$ is an optimized tree-level value with the minimum delay and high regularity. The simulation results of adaptive equalization applying the LMS structure, an efficient systolic DLMS structure using an optimized tree-level rule, and the conventional DLMS structure are shown in Fig. 6. Each learning curve is obtained by averaging the instantaneous squared error curve with 200 runs. In Fig. 6, the proposed efficient systolic DLMS architecture has similar convergence to that of the LMS structure. By contrast, the conventional DLMS structure has the largest convergence fluctuation among the three structures.

In the second application, we apply the efficient systolic architecture and rule to system identification [2] as shown in Fig. 7 by computer simulation. The adaptive transversal filter containing 16 taps (i.e., $N = 16$) identifies the unknown system. The unknown system is a 10-tap bandpass FIR filter, whose impulse response is given as

$$h_n = \begin{cases} \dfrac{\sin(\hat{w}_H(n-4.5))}{\pi(n-4.5)} \\ \quad -\dfrac{\sin(\hat{w}_L(n-4.5))}{\pi(n-4.5)}, & n=0,\,1,\,2,\,\ldots,\,9 \\ 0, & \text{otherwise} \end{cases} \tag{9}$$

where $\hat{w}_H$ and $\hat{w}_L$ denote the high and low edges of the passband, respectively, and we choose $\hat{w}_H = 0.7\pi$ and $\hat{w}_L = 0.3\pi$ for simulation. The input sequence is the white Gaussian random process of zero mean and unit variance. Assume $p_{\max} = 4$ and $\mu = 0.05$. Through the optimized tree-level rule, $p = 2$, 3, and 4 lead to $\{D, N_p\} = \{7, 1\}$, $\{6, 1\}$, and $\{6, 1\}$, respectively. As previously described, the rule shows that $p = 2$ and $p = 3$ both are the optimized tree-level values for this architecture with minimum delay and high regularity. The simulation results of system identification applying (a) LMS structure, (b) efficient systolic DLMS structure using an optimized tree-level rule, and (c) conventional DLMS structure are shown in Fig. 8, where the ensemble average is carried out with 50 runs. As a

consequence, the convergence rate of (b) is superior to that of (c) by computer simulation.

V. Conclusion

An efficient N-tap systolic DLMS adaptive FIR digital filter utilizing a new tree-systolic PE has been presented in this paper. Under the maximum driving constraint of the feedback error signal, the practical rule to decide the optimized tree level value without sacrificing the systolic characteristics is provided. Finally, we verify our systolic-array architecture via simulation of adaptive equalization and system identification applications. This efficient architecture amenable to VLSI implementation furnishes the same lowest critical period as that in [5], with finite driving, local connections, and satisfactory convergence at no extra area cost.

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