Front-End Amplifier of Low-Noise and Tunable BW/Gain for Portable Biomedical Signal Acquisition

[1]Chun-Chieh Huang, [1]Shao-Hang Hung, [1]Jen-Feng Chung
[1]Department of Electrical and Control Engineering
National Chiao Tung University
Hsinchu, Taiwan
siegfi.iic93g@nctu.edu.tw

Lan-Da Van, Chin-Teng Lin, *Fellow, IEEE*
[2]Department of Computer Science
National Chiao Tung University
Hsinchu, Taiwan
ldvan@cs.nctu.edu.tw

***Abstract*—**We proposed a novel analog circuit design which is suitable for various biomedical signal acquisitions. In addition to the consideration of low power and low noise, the analog front-end integrated circuit (AFEIC) is presented with design of high common-mode rejection ratio (CMRR) and high power supply ripple rejection ratio (PSRR). It has not only reduced the number of outer components, and enhances a better signal-to-noise ratio (SNR). The chip includes a current-balancing instrumentation amplifier, switched-capacitor filter, non-overlapping clock generator, and a programmable gain amplifier (PGA). It was fabricated by TSMC 0.35 μm CMOS 2P4M standard process, with CMRR 155 dB CMRR, 131 dB of PSRR+, and 127 dB of PSRR- at 50 Hz. The power consumption is about 142.4 μW under ±1.5V supply.

I. INTRODUCTION

The development of the biomedical recording system have been created many years. Due to the weak amplitude characteristic, biomedical signals are easy to be influenced by the test patterns, environment, and devices, etc. For above reasons, general small scale physiology scholar purchase commercialized bio-signal recording devices to analyze the signals. Examined persons are connected to a bulky and mains-powered instrument generally, which reduces their mobility and makes them uneasy. Also this will influence the recoding data and analysis result. Therefore, there is a growing demand for low-power, small size, and ambulatory bio-signal acquisition system.

Figure 1 shows the frequency characteristics of various biomedical signals such as EGG, ERG, blood pressure, EOG, EEG, ECG, EMG, ENG, and PCG. Due to the low frequency and μV level amplitude of these signals, in-band noise of the AFEIC is dominated by 1/f noise. Moreover, amplitude and frequency characteristics of biomedical signals are various for different application. Therefore, the digital controllable interface for selectable gain and bandwidth is integrated should also design and integrate into the system.

This work was supported in part by the National Science Council (NSC) Grant NSC-96-2221-E-009-220, MOEA-96-EC-17-A-01-S1-048, and NSC-96-2220-E-009-038.

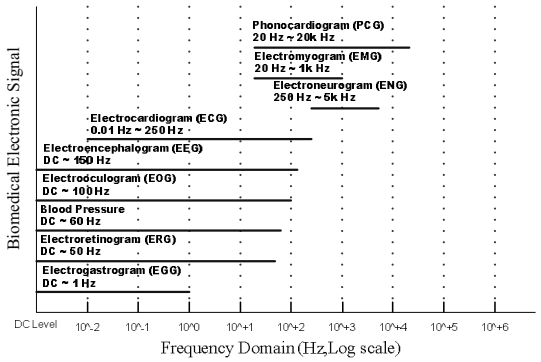

Figure 1. Frequency characteristics of various biomedical signals.

This paper proposes a novel AFEIC design with low noise, low power, and high gain, high CMRR as well as high PSRR simultaneously. In Addition, the tunable characteristic of gain and bandwidth is suitable for various biomedical signals.

We give an introduction on the analog front-end block on Section II. On Section III describes the architecture of the proposed AFEIC and the design of its individual block system. The experimental results and discussions are presented in Section IV, and have conclusions on Section V finally.

II. ANALOG FRONT-END ARCHITECTURE OVERVIEW

The biomedical signals should be processed by three procedures before back-end system by analog-to-digital converter. They are instrumentation amplifier (IA), low-pass filter, and gain stage amplifier. Besides, several signals we've shown in Fig. 1 were distributed at low-band frequency. Hence, general front-end systems were realized with extensive passive components to suit for bio-signal request. Due to layout and cost issue, we can integrate the passive elements in chips via CMOS technology. Further more, the system needs to support growing of the channel numbers, and the bulky size will be if they still use extensive elements. To overcome these problems, the first goal of proposed AFEIC d

is to integrate system into a single chip including passive elements. Second, configurability on gain and bandwidth for different biomedical signals is necessary to be controlled by digitized controller.

Figure 2 shows the architecture of the analog front-end IC for the acquisition of various biomedical signals. The readout channel of the system consists of the current-balancing instrumentation amplifier (CBIA), a switched-capacitor filter (SCF), a non-overlapping clock generator, a PGA.

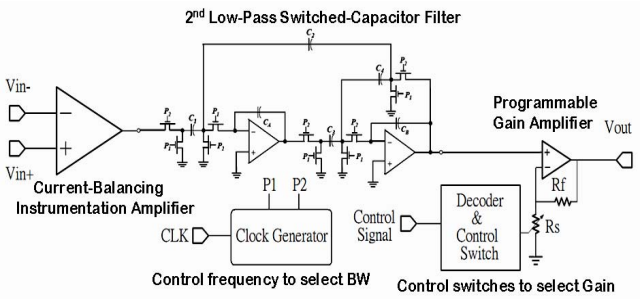

Figure 2. Architecture of the analog front-end circuit design.

A current feedback technique for IA design is applied to the analog front-end circuit system in this paper. The AFEIC for portable biomedical applications is presented with ±1.5V supply offering a high CMRR, PSRR, and acceptable low input-referred noise. Being powered with two 1.5-V button cell batteries without using any external components, the gain of the AFEIC is set to minimum 52.66 dB and maximum 80.45 dB. Additionally, a built-in digital interface provides the capability to control the functions with selectable system bandwidth and voltage gain.

III. Design and Implementation of Proposed AFEIC

A. Current-Balancing Instrumentation Amplifier(CBIA)

Conventional resistive feedback differential amplifiers used for voltage-mode instrumentation amplifiers. Including the classical structure, it is not suitable for the system on requirements such as low power, low cost, high CMRR and high PSRR. To attach these goals, amplifiers have to be designed with low output impendence to drive the feedback resistors, which implies high currents and large power drain. At the mean time, they also need low mismatch resistors to achieve high CMRR. It usually requires laser trimmed resistors, which is expensive and not available in a CMOS process. One solution for this problem is current feedback instrumentation amplifiers [1]-[5].

Due to CMRR improvement on IA , instead of simple current mirror architecture, a high-swing cascade current mirror is used. It may increase the output resistance of the mirror without deteriorating the DC behavior of the entire circuit. Output resistance of the mirror is very important because it makes up the tail resistance of the input differential pair, which plays a fundamental role to determine the CMRR of the amplifier. Consequently, the most important feature of CBIA is CMRR improved with this high-swing cascade circuit. The schematic of our design is shown in Fig. 3.

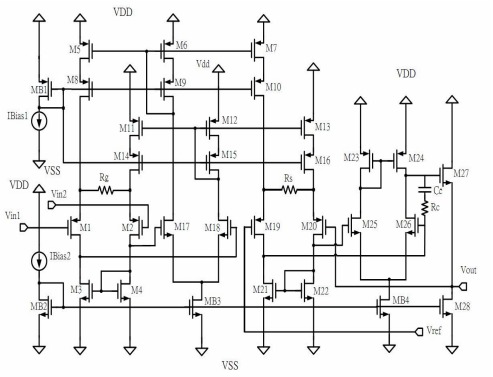

Figure 3. Schematic of the current-balancing instrumentation amplifier with CMRR improved.

B. Switched-Capacitor Low-Pass Filter

Switched-capacitor (SC) filters have become extremely popular due to their accurate frequency response, linearity, and dynamic range. Since coefficients of SC filters are determined by capacitance ratios which can be set precisely in ICs (on the order of 0.1%), accuracy of SC filters are much better than RC filters (as much as 20%).

Before designing the specification of the switched-capacitor low-pass filter, the system bandwidth should be set up in advance. EEG signals distribute form DC to 150 Hz, and we need a low-pass filter which can filter the upper bound noise higher than 150 Hz. The reason why the filter is implemented with the switched-capacitor (SC) configuration is the consideration for system on chip (SoC) and low-cost issue. If we design general active/ passive filters to realize the system bandwidth to such quite low frequency (150 Hz), a great deal of chip layout area is needed, especially for capacitors and resistors. Owing to above-mentioned reasons, they are not proper to be applied for biomedical signal acquisition application with such quite low distributing frequency.

Figure 4 shows the architecture of the switched-capacitor low-pass bi-quad filter. We set up the switching frequency and chose with proper values to fit what system designed. For fixed-value sampling capacitors, they could be arranged with different switching clocks to realize different equivalent resistors to reach various filtering bandwidth suite for various kinds of biomedical signals. In other words, the filter could easily arriver the target of selectable bandwidths with different digital switching clocks for multi bio-signal acquisition application.

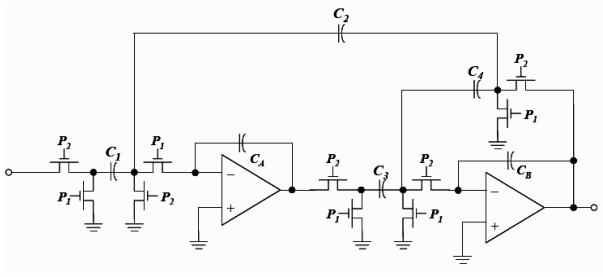

Figure 4. Architecture of the switched-capacitor low-pass biquad filter with sharing switches.

C. *Programmable Gain Filter*

The programmable gain amplifier shown in Fig. 5 provides further amplification with respect to the current-balancing instrumentation amplifier. To prevent the input impedance of the amplifier from loading the output current-balancing IA, a non-inverting configuration is used. By digital selecting the input signal of the 2-to-4 decoder to connect the resistors via NMOS switches, the amplifier provides programmable voltage gain of 0, 11, 18.4, 27.8 dB.

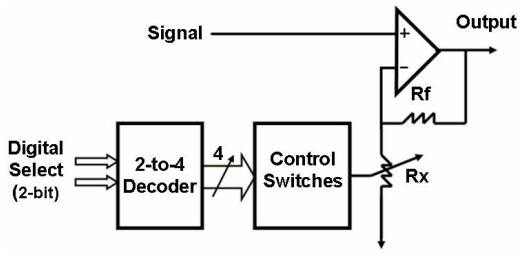

Figure 5. Architecture of the programmable gain filter.

IV. RESULTS AND DISCUSSIONS

The AFE IC is fabricated using TSMC 0.35-µm CMOS 2P4M standard process. The chip occupies an area of $0.907\times1.129mm^2$, as shown in complete layout of AFE IC in Fig. 6, the floor plan of the chip employs mixed-signal layout techniques [9] to minimize the digital signals from disturbing the sensitive analog signals.

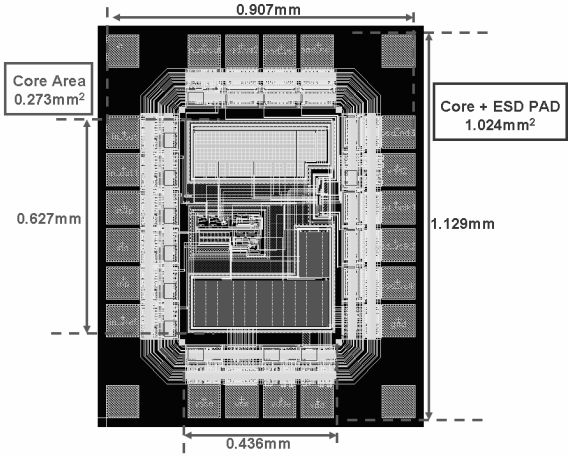

Figure 6. Layout of complete AEF IC including ESD PADs.

The most important block building of the analog front-end system is CBIA. It defines the noise performance, the CMRR, and the PSRR of the analog front-end. Fig. 7 shows the frequency response of the CBIA, and it provides fixed voltage gain of 52.6 dB below the frequency of CMRR, PSRR+ and PSRR- of the CBIA are shown in Figs. 8, 9, and 10, respectively. The CMRR performance of the AFE IC is at least 130 dB from DC to 1k Hz, and this is more than sufficient for biomedical signals acquisition requirements owing to most bio-signal bandwidths are much lower than 1k Hz.

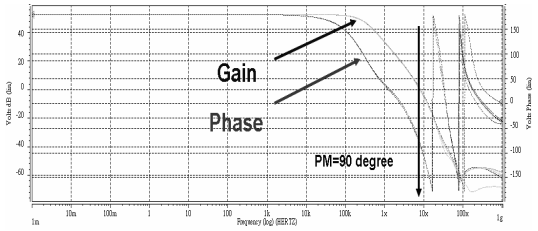

Figure 7. Frequency response of current-balancing IA.

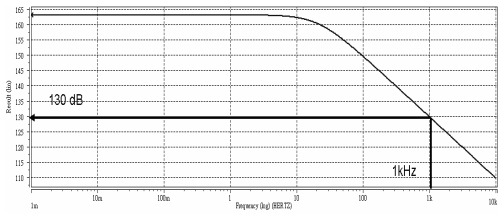

Figure 8. CMRR performance of the current-balancing IA.

For verifying the programmable gain capability of the AFE IC, Fig. 11 shows the possible gain of the PGA. According to above results, the AFE IC gain can be programmed from 52.6 dB to a maximum of 80.4dB. With the wide range of programmable gain, the AFE IC is capable of amplifying various biomedical signals, such as EEG, EMG, EOG, and ECG.

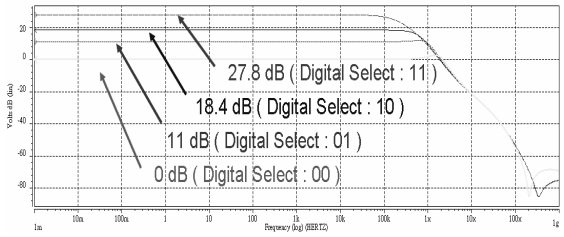

Figure 9. Frequency response of current-balancing IA.

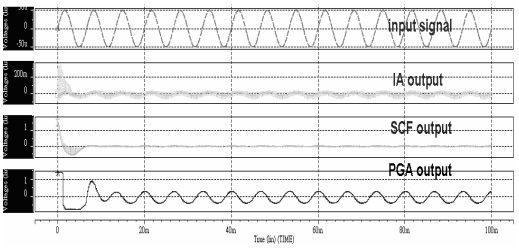

Figure 10. Transient response in Case 1: simulation for EEG characteristics.

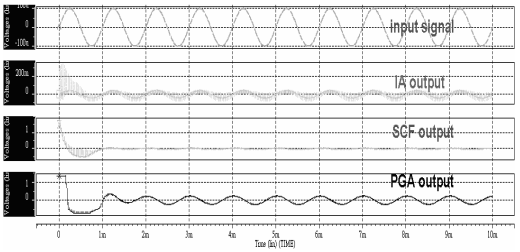

Figure 11. Transient response in Case 2: simulation for EMG characteristics.

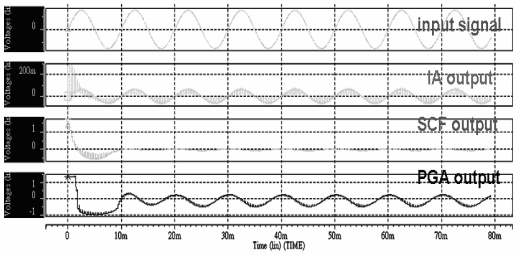

Figure 12. Transient response in Case 3: simulation for EOG characteristics.

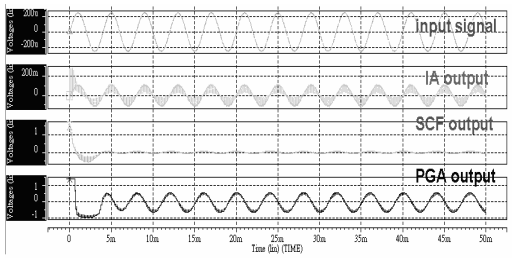

Figure 13. Transient response in Case 4: simulation for ECG characteristics.

Table I summarizes the comparison of the parameters of this AFE IC with those of reported AFEIC works. It can be seen that the proposed AFE IC offers technical merits of reasonable low power and high CMRR, PSRR+ and PSRR- performance. In addition, the present AFE IC is fully implemented into a signal with relative small size. By integrated with digital interface, the AFE IC has selectable system gain and bandwidth.

TABLE I. PERFORMANCE COMPARISON WITH OTHER PUBLICATIONS

Parameters	Ref [9] 1998	Ref [10] 2005	Ref [11] 2007	This Work
CMOS Technology	2.4um	0.5um	0.5um	0.35um
Supply (V)	9	± 1.5	3	± 1.5
No. of Channels	16	1	1	1
Core Area (mm^2)	24	4.81	1.95	0.273
Mid-Band Gain (dB)	Up to 74	0 ~ 80	51.82 ~ 67.96	52.66 ~ 80.45
Current Consumption per Channel (uA)	520	485	20	47.468
Bandwidth (Hz)	0.3 ~ 150	0.3 ~ 150	Selectable	Selectable
Input Common Mode Range (V)	-3.8 ~ 1.5	-1.5 ~ 1.3	1.05 ~ 1.7	-1.4 ~ 0.33
Input Referred Noise (uVrms) (0.3Hz<BW<150Hz)	1.39	0.86	< 0.7	2.417
CMRR @ 50Hz (dB)	99	117	> 120	155
PSRR+ (dB)	40 @10Hz	65 @10Hz	80 @50Hz	131 @50Hz
PSRR- (dB)	-	52 @10Hz	78 @50Hz	127 @50Hz

V. CONCLUSIONS

The AFEIC is realized on a signal chip without any external device and offers benefits in terms of smaller size, low power consumption, high CMRR, and high PSRR. It is suitable for portable system with multi bio-signals such as EEG, EMG, EOG, ECG, for its programmable functions on gain and bandwidth. The proposed input stage of the current-balancing IA achieves 155 dB CMRR, 131 dB PSRR+ and 127 dB PSRR- at the frequency of 50 Hz.

ACKNOWLEDGMENT

This work was supported in part by the National Science Council (NSC) Grant NSC-96-2221-E-009-220, MOEA-96-EC-17-A-01-S1-048, and NSC-96-2220-E-009-038.

REFERENCES

[1] H. Krabbe, "A high performance monolithic instrumentation amplifier," *Proc. in ISSCC Dig. Tech. Papers*, pp. 186-187, Feb. 1971.

[2] A. P. Brokaw and M. P. Timko, "An improved monolithic instrumentation amplifier," *IEEE J. Solid-State Circuits,* vol. SC-10, pp. 417-423, Dec. 1975.

[3] R. Van De Plassche, "A wide-band monolithic instrumentation amplifier," *IEEE J. Solid-State Circuits,* vol. SC-10, pp. 424-431, Dec.1975.

[4] M. S. J. Steyaert, W. M. C. Sansen, and C. Zhongyuan, "A micropower low-noise monolithic instrumentation amplifier for medical purposes," *IEEE J. Solid-State Circuits,* vol. SC-22, pp. 1163-1168, Dec. 1987.

[5] C. Toumazou and F. J. Lidgey, "Novel current-mode instrumentation amplifier," *Electron. Lett.* vol. 25, no. 3, Feb. 1989.

[6] E. A. Vittoz, Micropower Techniques, in Design of MOS VLSI Circuits for Telecommunications, Y. Tsividis and P. Antognetti, Eds. Englewood Cliffs, NJ: Prentice Hall, 1985.

[7] Honglei Wu and Yong-ping Xu, "A low-voltage low-noise CMOS instrumentation amplifier for portable medical monitoring systems," *IEEE-NEWCAS Conference*, pp.295-298, 19-22 June, 2005.

[8] C. Jakobson, I. Bloom, and Y. Nemirovsky, "1/f noise in CMOS transistors for analog applications from subthreshold to saturation," *Solid-State Electron*., vol. 42, no. 10, pp. 1807-1817, 1998

[9] Rui Martins, Siegfried Selberherr, and Francisco A. Vaz, "A CMOS IC for portable EEG acquisition systems," *IEEE Transactions on Instrumentation and Measurement*, Vol. 47, No. 5, Oct. 1998.

[10] K. A. Ng and P. K. Chan, "A CMOS Analog Front-End IC for Portable EEG/ECG Monitoring Applications," *IEEE Transactions on Circuits and Systems—I*: Regular Papers, Vol. 52, No. 11, Nov. 2005.

[11] Refet Firat Yazicioglu, Patrick Merken, Robert Puers, and Chris Van Hoof, "A 60uW 60nV/ √Hz readout front-end for portable biopotential acquisition systems," *IEEE Journal of Solid-State Circuit*, Vol. 42, No. 5, May 2007.

[12] R.F. Yazicioglu, P. Merken and C. Van Hoof, "Integrated low-power 24-channel EEG front-end," *Electronics Letters 14th,* Vol. 41 No. 8, April 2005.

[13] Paulo Augusto Dal Fabbro and Carlos A. dos Reis Filho, "An Integrated CMOS Instrumentation Amplifier with Improved CMRR," *IEEE Proceeding of the 15th Symposium on Integrated Circuits and Systems Design*, 2002.

[14] Refet Firat Yazicioglo, Patrick Merken, Chris Van Hoof, "Effect of Electrode Offset On the CMRR of the Current Balancing Instrumentation Amplifiers," *Research in Microelectronics and Electronics*, Vol.1, pp.35-38, 2005.

[15] D. C. Von Grunigen, R. Sigg, M. Ludwig, U. W. Brugger, G. S. Moschytz, H. Melchior, "Integrated Switched-Capacitor Low-Pass Filter with Combined Anti-Aliasing Decimation Filter for Low Frequencies," *IEEE J. Solid-State Circuits*, Vol. SC-17, pp. 1024-1028, Dec. 1982.