A New VLSI 2-D Diagonal-Symmetry Filter Architecture Design

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***Abstract*—In this paper, we propose two new two-dimensional (2-D) IIR and FIR filter architectures for 2-D transfer function with diagonal symmetry. The presented type-I structure with diagonal symmetry has the lowest number of multipliers, and zero latency without sacrificing the number of the delay elements. Importantly, the proposed type-II IIR filter possesses high speed, local broadcast, and the same number of multipliers and latency as the type I shows at expense of a slight increment of number of delay elements.**

I. INTRODUCTION

Recently, 2-D digital filters are widely applied in a variety of digital signal processing (DSP) systems such as image restoration [1] obtained through a 2-D low-pass intraframe filter, image enhancement [2, 3] performed by a 2-D high-pass filter and bio-medical signal processing [4]. Generally speaking, the category of 2-D digital filters can be divided into IIR and FIR digital filters. By contrast, an IIR digital filter has the advantage of highly computational efficiency and low hardware cost. An FIR digital filter has the merit of stable and linear-phase properties. Although 2-D digital filters can be simulated on a general-purpose computer, it seems unlikely to process input signals in real time due to a large amount of computation. Therefore, an application-specific integrated circuit (ASIC) design plays an important role for the realization of 2-D digital filters. Using ASIC approach, the throughput rate and cost can be easily sped up and alleviated, respectively. Several 2-D filter VLSI architectures have been existed in [7-11]. However, the existing ASIC approaches have not been applied to design 2-D transfer function possessing certain frequency response symmetries. On the other hand, the hardware evaluation metrics have not yet been debated. Thus, we are motivated to propose one new 2-D IIR and FIR filter with less number of multipliers using diagonal symmetry property [5, 6]. It is known that 2-D frequency responses possess many types of symmetries that can be used to reduce the design complexity and the implementation. In this paper, we choose diagonal symmetry scheme to determine 2-D VLSI architecture. Note that when the frequency response has no symmetry, there is a technique to decompose that frequency response into components each of which has the desired symmetry. As a consequence, there is a motivation to derive the 2-D diagonal-symmetry IIR and FIR filter architecture designs.

The structure of this paper is organized as follows. The brief review of diagonal symmetries is presented in Section II. The proposed 2-D diagonal-symmetry IIR and FIR filter architectures are discussed in Section III. In Section IV, the comparison results are tabulated in terms of the number of multipliers as well as delay elements, critical period, latency, and whether the local broadcast exists. In the last section, concise statements conclude this presentation.

II. REVIW OF DIAGONAL SYMMETRY

2-D frequency responses possess many types of symmetries and the presence of these symmetries can be used to reduce the design complexity of these filters. Symmetry in a frequency response induces certain constraints on the coefficients of filter transfer function which in turn reduces the filter design complexity. In the following, the diagonal symmetry constraints on polynomials are reviewed.

For a 2-D z-domain polynomial $Q(z_1, z_2)$, we can represent the magnitude squared function of the frequency response in the form

$$F(\theta_1,\theta_2) = Q(e^{j\theta_1}, e^{j\theta_2}) \cdot Q^*(e^{-j\theta_1}, e^{-j\theta_2})$$

$$= Q(z_1, z_2) \cdot Q^*(z_1^{-1}, z_2^{-1})\,|_{z_i = z^{j\theta_i}}, \text{for } i = 1, 2 \qquad (1)$$

Where Q^* is obtained by complex conjugating the coefficients of Q. A magnitude squared function of the frequency response with diagonal symmetry can be defined as

$$F(\theta_1,\theta_2) = F(\theta_2,\theta_1)$$
$$= F(-\theta_1,-\theta_2) = F(-\theta_2,-\theta_1) \quad ,\forall(\theta_1,\theta_2) \qquad (2)$$

Since real polynomials always satisfy $F(\theta_1, \theta_2) = F(-\theta_1, -\theta_2)$, $F(\theta_1, \theta_2) = F(\theta_2, \theta_1)$ is enough to ensure the diagonal symmetry. Using the magnitude squared function in

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(1) and diagonal symmetry definition in (2), we can conclude the following factors with diagonal symmetry in their magnitude responses [5]:

$$Factor1 = Q_1(z_1, z_2) \tag{3a}$$

$$\begin{aligned} Factor2 = {} & Q_2(x_1, x_2) + y_1 y_2 Q_3(x_1, x_2) \\ & + y_1 Q_4(x_1, x_2) - y_2 Q_4(x_2, x_1) \end{aligned} \tag{3b}$$

$$Factor3 = Q(z_1, z_2) \cdot Q(z_2, z_1) \tag{3c}$$

$$Factor4 = Q(z_1, z_2) \cdot Q(z_2^{-1}, z_1^{-1}) \tag{3d}$$

Where $Q_1(z_1, z_2) = Q_1(z_2, z_1)$, $Q_k(x_1, x_2) = Q_k(x_2, x_1)$ for k=2, 3, and $x_i = z_i + z_i^{-1}$, $y_i = z_i - z_i^{-1}$ for i=1, 2.

Now, using the diagonal symmetry constraints on polynomial factors, a procedure to design a 2-D IIR and FIR digital filter architectures is presented in the next section.

III. 2-D DIAGONAL-SYMMETRY DIGITAL FILTER ARCHITECTURE

In this section, we propose two new 2-D diagonal-symmetry IIR and FIR digital filter architectures. These architectures commonly improve the number of multipliers and occupy zero latency as well. The general transfer function of a 2-D IIR digital filter can be represented as

$$H(z_1, z_2) = \frac{\sum_{i=0}^{N_1}\sum_{j=0}^{N_2} a_{i,j} z_1^{-i} z_2^{-j}}{\sum_{i=0}^{N_1}\sum_{j=0}^{N_2} b_{i,j} z_1^{-i} z_2^{-j}} = \frac{N(z_1, z_2)}{D(z_1, z_2)} \tag{4}$$

where $b_{0,0} = 1$, $a_{i,j}$ as well as $b_{i,j}$ and $N_1 \times N_2$ are coefficients and the order of the IIR digital filter, respectively. Throughout this paper, a square image $M \times M$ is fed to the following structures in raster-scan mode, and thus the delay $z_2^{-1} = z^{-1}$ and $z_1^{-1} = z^{-M}$, where z^{-1} and M denote a unit delay element and the width of an image, respectively. Since each $N(z_1, z_2)$ and $D(z_1, z_2)$ possess diagonal symmetry property discussed above for Q, we decide the numerator to be $N(z_1, z_2) = N(z_2, z_1)$ and the denominator to be $D(z_1, z_2) = D(z_2, z_1)$, which is the diagonal symmetry condition in (3a). As a representative example, we perform and deduce the order of structures under an assumption $N_1 = N_2 = 2$. The following are the forms for the numerator and denominator in (5a) and (5b). It can be seen that the coefficient matrices of numerator and denominator both have diagonal symmetry. As a result, the number of variables to implement is reduced from 17 (9 for the numerator and 8 for the denominator) to 11 (6 for the numerator and 5 for the denominator), and attain multiplier reduction by 35.3%.

$$N(z_1, z_2) = \begin{array}{c} \\ z_1^0 \\ z_1^{-1} \\ z_1^{-2} \end{array} \begin{array}{c} \begin{array}{ccc} z_2^0 & z_2^{-1} & z_2^{-2} \end{array} \\ \begin{bmatrix} \boxed{a_{00}} & a_{01} & a_{02} \\ \boxed{a_{10}} & \boxed{a_{11}} & a_{12} \\ \boxed{a_{20}} & \boxed{a_{21}} & \boxed{a_{22}} \end{bmatrix} \end{array} \tag{5a}$$

$$D(z_1, z_2) = \begin{array}{c} \\ z_1^0 \\ z_1^{-1} \\ z_1^{-2} \end{array} \begin{array}{c} \begin{array}{ccc} z_2^0 & z_2^{-1} & z_2^{-2} \end{array} \\ \begin{bmatrix} \boxed{1} & b_{01} & b_{02} \\ \boxed{b_{10}} & \boxed{b_{11}} & b_{12} \\ \boxed{b_{20}} & \boxed{b_{21}} & \boxed{b_{22}} \end{bmatrix} \end{array} \tag{5b}$$

Initially, we can express (4) for $N_1 = N_2 = 2$ as follows.

$$Y = \sum_{i=0}^{2}\sum_{j=0}^{2} a_{i,j} z_1^{-i} z_2^{-j}(X) - \sum_{i=0}^{2}\sum_{\substack{j=0 \\ i+j\neq 0}}^{2} b_{i,j} z_1^{-i} z_2^{-j}(Y) \tag{6}$$

where $X = X(z_1, z_2)$ and $Y = Y(z_1, z_2)$ are defined as input and output of the digital filter, respectively. Due to the diagonal symmetry property in (5a) and (5b), we recast (6) using register reordering in (7)

$$\begin{aligned} Y = {} & \sum_{i=0}^{2} z_1^{-i} z_2^{i\times P}(a_{i,i} z_2^{-i}) z_2^{-i\times P} X - \sum_{i=1}^{2} z_1^{-i} z_2^{i\times P}(b_{i,i} z_2^{-i}) z_2^{-i\times P} Y \\ & + \sum_{i=0}^{1}\sum_{j=i+1}^{2} a_{i,j}[z_1^{-i} z_2^{i\times P}(z_2^{-j} z_2^{-i\times P}) + z_1^{-j} z_2^{j\times P}(z_2^{-i} z_2^{-j\times P})]X \\ & - \sum_{i=0}^{1}\sum_{j=i+1}^{2} b_{i,j}[z_1^{-i} z_2^{i\times P}(z_2^{-j} z_2^{-i\times P}) + z_1^{-j} z_2^{j\times P}(z_2^{-i} z_2^{-j\times P})]Y \end{aligned} \tag{7}$$

Where integer variable P is restricted in range of 0 and M. Since the image is in the raster scan of this paper, the delay $z_2^{-1} = z^{-1}$ and the delay $z_1^{-1} = z^{-M}$ are realized by a unit delay element and a shift-register (SR) with size of M, respectively. Thus, the terms of $z_1^{-i} z_2^{i\times P} = z_2^{-i(M-P)}$ can be implemented by the number of (*M*-*P*) shift registers. Next, we deduce two VLSI architectures with respect to *P*=0 and *P*=1.

◆ Type I with *P*=0:

Equation (7) can be expressed in (8).

$$\begin{aligned} Y = {} & \sum_{i=0}^{2} a_{i,i} z_1^{-i} z_2^{-i} X - \sum_{i=1}^{2} b_{i,i} z_1^{-i} z_2^{-i} Y \\ & + \sum_{i=0}^{1}\sum_{j=i+1}^{2} a_{i,j}[z_1^{-i} z_2^{-j} + z_1^{-j} z_2^{-i}]X - \sum_{i=0}^{1}\sum_{j=i+1}^{2} b_{i,j}[z_1^{-i} z_2^{-j} + z_1^{-j} z_2^{-i}]Y \end{aligned} \tag{8}$$

Equation (8) can be mapped onto the diagonal symmetry IIR filter architecture as depicted in Fig. 1. In addition, the users merely set $b_{i,j}$ to zero except b_{00}=1 such that a new diagonal-symmetry FIR filter architecture as shown in Fig. 2 can be obtained. In this case, although the proposed type-I IIR filter has the lowest number of multipliers, the larger critical period and global broadcast are incurred. Thus, we are motivated to

derive another type filter with less critical period and local broadcast.

◆ Type II with P=1:

Observing the architectures in Fig. 1 and Fig. 2, we find that the critical period is larger and the input and output signals are globally broadcast. It is harmful to the limited fanout VLSI design. In order to enhance this architecture with higher speed and local broadcast, we set P=1 in (9).

$$\begin{aligned} Y = &\sum_{i=0}^{2} z_1^{-i} z_2^{i}(a_{i,i} z_2^{-2i})X - \sum_{i=1}^{2} z_1^{-i} z_2^{i}(b_{i,i} z_2^{-2i})Y \\ &+ \sum_{i=0}^{1}\sum_{j=i+1}^{2} a_{i,j}[z_1^{-i} z_2^{i}(z_2^{-j} z_2^{-i}) + z_1^{-j} z_2^{j}(z_2^{-i} z_2^{-j})]X \\ &- \sum_{i=0}^{1}\sum_{j=i+1}^{2} b_{i,j}[z_1^{-i} z_2^{i}(z_2^{-j} z_2^{-i}) + z_1^{-j} z_2^{j}(z_2^{-i} z_2^{-j})]Y \end{aligned} \tag{9}$$

In similar behaviors, the resulting diagonal-symmetry IIR architecture corresponding to (9) is shown in Fig. 3. In addition, we can also obtain a new diagonal-symmetry FIR filter architecture in Fig. 4 by setting $b_{i,j}$ to zero except b_{00}=1.

IV. Comparison Results of IIR and FIR Digital Filters

In this section, the comprehensive comparison results of IIR and FIR filter architectures are tabulated in Table 1 and 2, respectively. The contents are in terms of number of multipliers, number of delay elements, critical period, latency, and local broadcast, where each critical period is calculated by tree method. Here T_m and T_a represent the operation time required for the multiplier and adder, respectively. In Table 1, it is shown that the proposed type I and type II IIR filter architectures lead to the lowest number of multipliers than that of [7, 9, 11]. Among the proposed two type IIR filter architectures, the former has less number of delay elements and the latter has higher throughput and local broadcast. Analogously, we compare the performance of these FIR filters as listed in Table 2 after setting b_{ij} to zero except b_{00}=1. On average, the numbers of delay elements in these two FIR works are almost equal to that of [11], and less than that of [7, 9]. For the proposed second-order IIR and FIR filters, the reduction of number of multipliers can be achieved 35.3% and 33.3%, respectively. From Tables 1 and 2, we guarantee that the presented type-I structure with diagonal symmetry has the lowest number of multipliers, zero latency without sacrificing the number of the delay elements. Importantly, the proposed type-II IIR filter possesses high speed, local broadcast, and the same number of multipliers and latency as the type I shows at expense of a slight increment of number of delay elements.

V. Conclusion

Two new diagonal-symmetry architectures for the implementation of 2-D IIR and FIR digital filters have been presented. The proposed structures have the lowest number of multipliers, high throughput, and zero latency without scarifying the number of delay elements. In addition, the percentage of the reduction of number of multipliers is nearly 50% as N is large enough.

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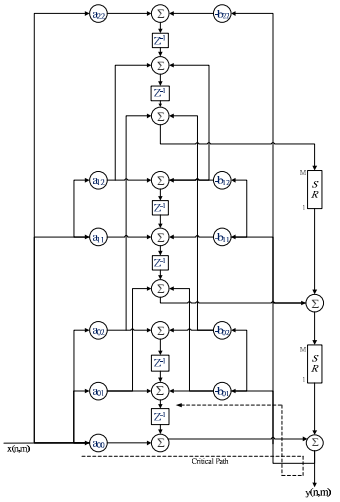

Figure 1. Proposed 2-D diagonal-symmetry IIR filter architecture with P=0.

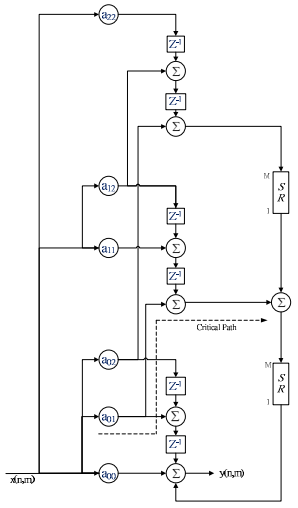

Figure 2. Proposed 2-D diagonal-symmetry FIR filter architecture with P=0.

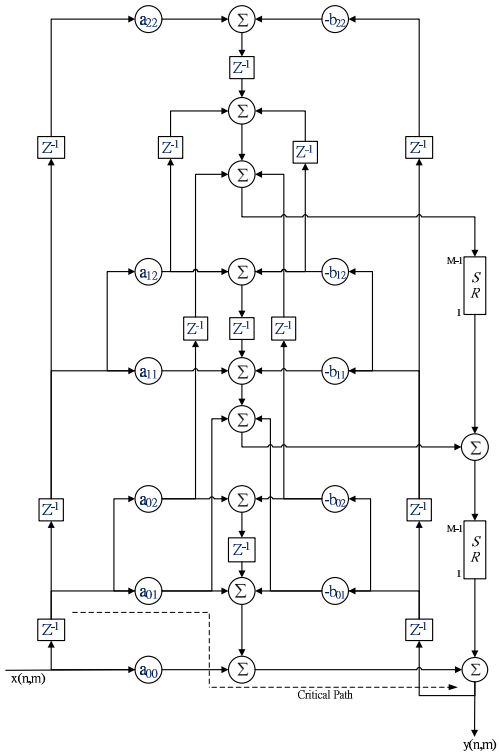

Figure 3. Proposed 2-D diagonal-symmetry IIR filter architecture with P=1.

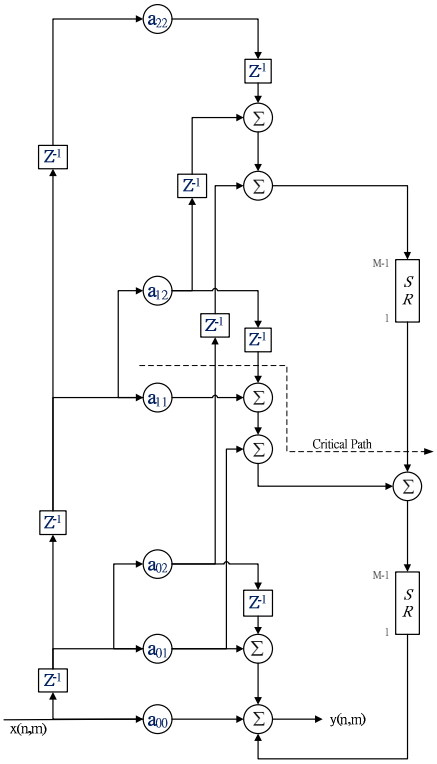

Figure 4. Proposed 2-D diagonal-symmetry FIR filter architecture with P=1.

Table 1 Comparison Results among the IIR Digital Filter Architecture for N=2

Parameter	Direct Form of M-S-P [7]	Ahmed [9]	Van [11]	This Work with P=0	This Work with P=1
No. of Multipliers	17	17	17	11	11
Critical Period	$2T_m+8T_a$	T_m+4T_a	T_m+3T_a	$2T_m+2T_a$	T_m+3T_a
Latency	0	1	0	0	0
Local Broadcast	No	No	Yes	No	Yes
No. of Delay Elements	6+3M	9+4M	9+2(P+M)	6+2M	11+2M

Table 2 Comparison Results among the FIR Digital Filter Architecture for N=2

Parameter	Direct Form of M-S-P [7]	Ahmed [9]	Van [11]	This Work with P=0	This Work with P=1
No. of Multipliers	9	9	9	6	6
Critical Period	T_m+4T_a	T_m+T_a	T_m+2T_a	T_m+T_a	T_m+2T_a
Latency	0	1	0	0	0
Local Broadcast	No	No	Yes	No	Yes
No. of Delay Elements	6+3M	9+2M	6+2M	6+2M	6+2M